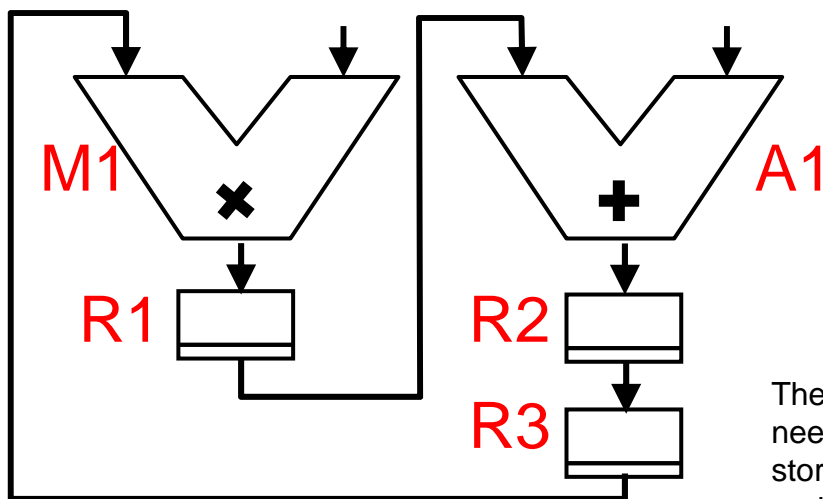


Question (related to the DFG after the look-ahead transformation): how is it possible that the cycle can be executed in 2 clock cycles while there are two delay elements in the loop and also clock cycles are spent in the computations?

Answer: delay elements are about timing at the data-flow level; they do not necessarily correspond to registers in the implementation.

To explain this, a data-path and a schedule are given below for the loop part of the DFG (exercise: complete the design for the entire DFG).



M1	m[n-2]	m[n-1]	m[n]		
A1	x[n-3]		x[n-2]		x[n]
R1	m[n-3]		m[n-2]	m[n-1]	m[n]
R2		x[n-3]		x[n-2]	x[n-1]
R3	x[n-4]	x[n-3]	x[n-2]		

The schedule has an iteration period of 2 clock cycles. The input register of an FU needs to have stable contents during the execution time of the FU (that is why R3 stores its contents for two clock cycles). R1 and R2 could be shared, saving 1 register at the expense of one multiplexer. Note that although m[n] and x[n-2] are conceptually 2 iterations, so 4 clock cycles, apart, in the realization, they are only separated by 2 clock cycles. This is due to the overlapped schedule.